# ABSTRACT

A system on a chip has functional blocks accommodated by at least one system bus, and an external bus for accommodating communication with external blocks. A single multi-jurisdictional bus arbiter has programmable rankings for assigning priorities to requests from blocks that are masters for either one of the both buses. Software and methods are also provided for assigning the priorities. The requests are analyzed with respect to which of the buses they require, and then priorities are assigned to maximize bus utilization, with increased speed for a system on a chip. In addition, a multi-jurisdictional multi-channel direct memory access block can be a master block for the system bus or the external bus.